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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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MCNEES, WALLACE & NURICK LLC 100 PINE STREET P.O. BOX 1166 HARRISBURG, PA 17108-1166				
			EXAMINER KIANNI, KAVEH C	
			ART UNIT 2883	PAPER NUMBER

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/605,638

Applicant(s)

RAHMAN, ANIS

Examiner

Kianni C. Kaveh

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2883

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-43 is/are pending in the application.
- 4a) Of the above claim(s) 36-41 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-25, 28-35, 42 and 43 is/are rejected.
- 7) ☒ Claim(s) 8, 26 and 27 is/are objected to.
- 8) ☒ Claim(s) 36-41 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 June 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 5.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 11-35 and 42-43, drawn to a photonic integrated circuit including a slab waveguide arrangement, classified in class 385, subclass 14.
- II. Claims 36-41, drawn to a method of fabricating a photonic integrated circuit including the steps of depositing and masking, classified in class 385, subclass 131.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case process of invention II can be used as optical router in an optical add/drop communication module rather than in an RAWG as in invention I.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Smith on 6/21/05 a provisional election was made without traverse to prosecute the invention of I, claims 11-35 and 42-43. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 36-41 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

Claim 18 is objected to because of the following informalities: a period at the end sentence is missing. Appropriate correction is required.

Claim Rejections - 35 USC 112

Claims 11, 24, 32, 34 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation 'said plurality of arrayed waveguides' in the 4th parag. of the claim. There is insufficient antecedent basis for this limitation in the claim.

Correction is required.

Claim 35 recites the limitations 'the modulator block' in the 2nd line of the claim. There is insufficient antecedent basis for this limitation in the claim. Correction is required.

claims 24, 32 and 34-35 are ambiguous, since 'waveguide amplifier block' is 'a 'waveguide amplifier block' and the claim language implies that 'the waveguide amplifier block is configured for connecting an external pump laser with the waveguide amplifier block through a wave guide interconnect' there are two separate elements 'waveguide amplifier block' and 'waveguide amplifier block'; also the analogous comparison of discrepancies is between an 'active unit' and a 'modulator block' as being separate units

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as claimed in claim 32; also the analogous comparison of discrepancies is between an 'photonic integrated circuit' and 'active unit' and/or 'the modulator block' as being separate units as claimed in claims 35 and 34. Corrections are required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the modulator for electro-optically processing output signals, as claimed in claim 28 which depends on claim 27, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Allowable Subject Matter

Claims 26-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if the base claim of these claims is no longer rejected under 35 USC 112.

Claims 26-27 are allowable because the prior art of record, taken alone or in combination, fails to disclose or render obvious wherein the amplifier block is comprised of a material that absorbs light in the 890 nanometer and the 1480 nanometer regions and emits light in the 1310 nanometer and 1550 nanometer regions in combination with the rest of the limitations of the base claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 11-25, 28-34, and 42-43 rejected under 35 U.S.C. 103(a) as being unpatentable over Takada et al. (US 6278813).

Regarding claim 11, 23- 24, 28-34 and 42-43, Takada teaches a second/third-phase optically integrated circuit (shown in at least fig. 24) comprising a monolithically integrated circuit (shown in at least fig. 31), comprising:

an input/output interface arranged on a substrate 1 comprising a plurality of waveguides 2 for simultaneously inputting at least one signal to and outputting at least one signal from the monolithically integrated circuit for demultiplexing a multiplexed optical signal in to n different constituent wavelengths and for combining n input optical signals composed of n different constituent wavelengths in to a multiplexed signal (shown in at least fig. 31, see also abstract and col. 2, 2nd parag.);

a slab waveguide 3 arranged on the substrate 1 having a first end and a second end, the first end coupled to the plurality of waveguides 2 of the input/output interface to focus the at least one input signal to the second end, and the second end coupled to the array of waveguides , for focusing the at least one output signal to the input/output interface through the first end (shown in at least fig. Item input/output waveguides and output signal being focused out of the slab 2nd end through output/input waveguides 2);

an array waveguide 93 arranged on the substrate 1 comprising a plurality of waveguides for coupling the one or more input signals (see waveguides in the area 88), separating the one or more input signals into the n different constituent wavelengths and focusing the n different constituent wavelengths back on to the slab 3 waveguide first end coupling to the input/output interface (shown in at least fig. 31, items waveguides coupling input light from the waveguides 2 through slab 3, and see col. 2, 2nd parag.), the plurality of waveguides of the array waveguide 93 being optically

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coupled at one end with the second end of the slab 3 waveguide, and terminated at the opposing end by the reflective mirror 87, each waveguide of said plurality of arrayed waveguides 93 having a predetermined path difference between successive waveguides (shown in at least fig. 31, items waveguides with different predetermined wavelengths), a reflective mirror 86 disposed at the opposing end of the array waveguide 93 for reflecting the one or more signals incident on it from the array waveguide 93 back into the array waveguide 93; and an active unit 22 formed on the substrate, the active unit connected to the photonic integrated circuit by a waveguide interconnect means (see at least col. 29, 1st parag. and col. 3, lines 38-43; wherein active unit is an array of photodiode formed on a perspective output waveguide array); a signal processing unit comprises a plurality of n electro-optical elements coupled to the photonic integrated circuit for electro-optically processing the input and output signals (see fig. 53, item signal processing elements/unit(s) 22 and/or 23);

However, Takada does not explicitly state that the above monolithically integrated circuit is a photonic integrated circuit; and that the above active unit is a waveguide amplifier and that the above signal processing unit is a modulator for interconnecting to an external optical device/pump laser. It is well known to those of ordinary skill in the art when the invention was made that a monolithically integrated circuit is known as a photonic integrated circuit and that it would have been obvious to a person of ordinary skill in the art when the invention was made to choose the above active device as a matter of further modification of signal an optical amplifier since such amplifier on an AWG circuit is conventional and that it would have been obvious to a

person of ordinary skill in the art when the invention was made to externally connect the above integrated circuit/RAWG to any external optical and/or non-optical device, such as a modulator or laser source, as a matter of further analyzing or processing the signal and since such interconnections are conventional, see the prior art of the record, and also suggested/implied by various embodiments by Takada, and since such optical integrated circuit enables accurately input/output desired frequencies and provide measurement without any loss (col. 11, 1st parag.).

Regarding claims 12-22 and 25, Takada further teaches wherein the active unit is selected from the group consisting of laser diodes, VCSELS, detector arrays and electro-optic modulators, receiver, transmitter, transceivers, and transponders (see at least col. 13, line 53; wherein also it is obvious to choose a frequency channel as a matter of choice); wherein any one of the waveguides of the input/output interface plurality of waveguides provides an input channel and a different waveguide of the input/output interface plurality of waveguides provides an output channel (shown in at least fig. 31, 33 and 21, items waveguides of input/output channel(s)); see also at least col. 25, last parag.+); wherein any one of the waveguides of the input/output interface plurality of waveguides provides an input channel and the remaining waveguides of the input/output interface plurality of waveguides are automatically output channels (shown in at least fig. 33, items waveguides of input/output/automatically output channels); wherein any one of the waveguides of the input/output interface plurality of waveguides provides an output channel and the remaining waveguides of the input/output interface

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plurality of waveguides are automatically input channels (shown in at least fig. 33, items waveguides of input/output/automatically output channels); wherein the one waveguide of the input/output interface is preselected as an input channel (shown in at least fig. 33, items waveguides of input/output preselected as input/output channel); wherein one of the plurality of waveguides of the input/output interface is an input and the remainder of the waveguides form output channels (shown in at least fig. 33, item #1 waveguide and output waveguides), and the number of output channels is n wherein n is selected from one of the group of integer numbers consisting of 4, 8, 12, 16, 24, 32, and 48 (see at least fig. 33, item Array waveguide grating 19 output with 4 output waveguides; wherein it is also obvious to choose any number of channels as a matter of choice); wherein one of the plurality of waveguides of the; input/output interface is an output and the remainder of the waveguides form input channels, and the number of input channels is n wherein n is selected from one of the group of integer numbers consisting of 4, 8, 12, 16, 24, 32, and 48 (see at least fig. 33, item Array waveguide grating 93 outputs with 1 input waveguide; wherein it is also obvious to choose any number of channels as input/output a matter of choice); wherein n waveguides of the plurality of input/output interface waveguides are spaced at a predetermined distance and form n channels (shown in at least fig. 33, item spaced waveguides with n channels); wherein the predetermined distance is selected from the group consisting of 0.25 nanometers, 0.4 nanometers, 0.8 nanometers, 1.6 nanometers, 4 nanometers, and 5 nanometers (see at least col. 2, line 10; wherein it is also obvious to choose channel spacing as matter of design choice); wherein n waveguides of the plurality of input/output interface

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waveguides form n channels, and the channel frequency is a predetermined frequency (see at least col. 8, 1st parag.); wherein the predetermined channel frequency is selected from the group consisting of about 31 GHz, and 50 GHz, 100 GHz, 200 GHz, 500 GHz, and 624 GHz (see at least col. 13, line 53; wherein also it is obvious to choose a frequency channel as a matter of choice).

Citation of Relevant Prior Art

Prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In accordance with MPEP 707.05 the following references are pertinent in rejection of this application since they provide substantially the same information disclosure as this patent does. These references are:

Inoue et al. 5546483 teaches at least independent claims including an optical amplifier

Kurokawa et al. 6456760 teaches modulator and amplifier in an AWAG/RAWG

Kurokawa et al. 6122419 teaches modulator and amplifier in an AWAG/RAWG

Purchase 200402086/21/05 17 teaches modulator/amplifier in an AWAG/RAWG

Dominic et al. 20050135778 teaches modulator/amplifier in an AWAG/RAWG

Katayama 6892003 teaches modulator/amplifier in an AWAG/RAWG

SEE ALSO at least other prior art provide by the applicant for obvious optical interfacing/units in AWG system.

These references are cited herein to show the relevance of the apparatus/methods taught within these references as prior art.

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Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to K. Cyrus Kianni whose telephone number is (571) 272-2417.

The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 6:00 p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font, can be reached at (571) 272-2415.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or:

Hand delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956.



K. Cyrus Kianni
Primary Patent Examiner
Group Art Unit 2883

June 24, 2005